# Bridging Hardware and Software Verification Witnesses

Dirk Beyer, Po-Chun Chien, and **Nian-Ze Lee**

LMU Munich, Germany

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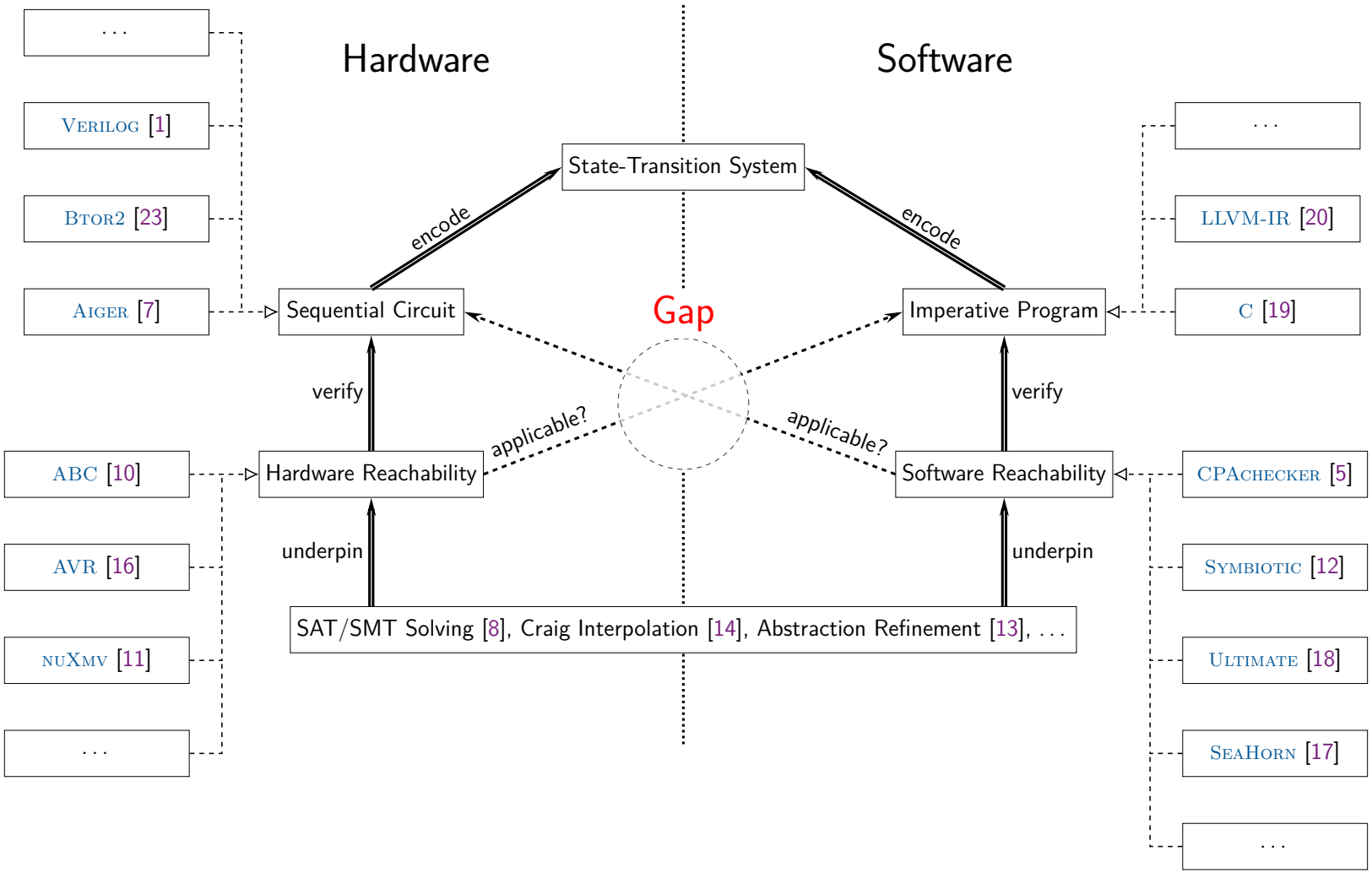
LMU LUDWIG-MAXIMILIANS-UNIVERSITÄT MÜNCHEN

SoSy-Lab Software Systems

# Closing the Gap between HW and SW Analysis



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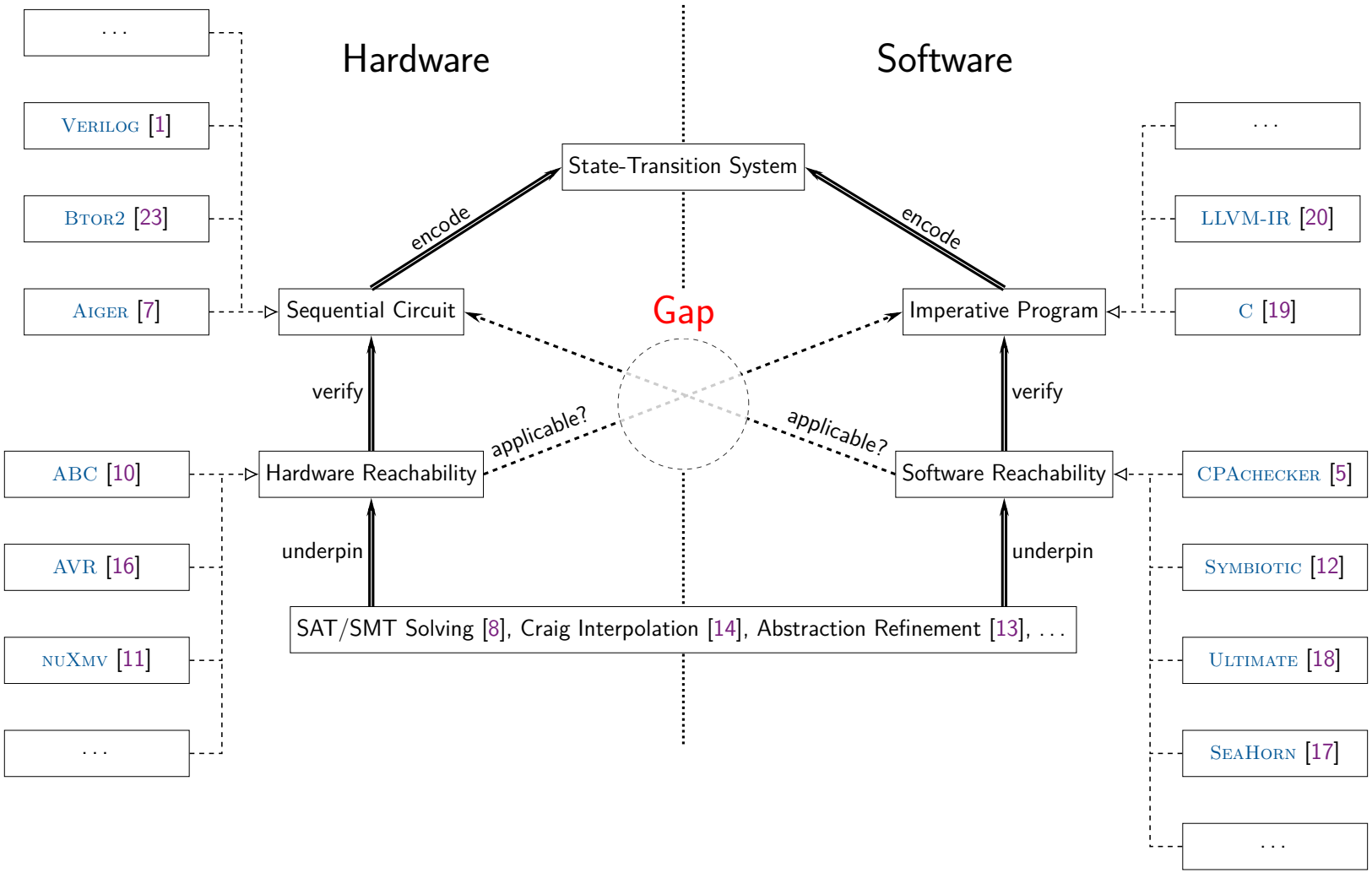


- Information exchange and explainability via **Witnesses**

# Outline

1. The Btor2 Language and Btor2C
2. Translating Software Witnesses to Btor2
3. Discussion

# The BTOR2 Language

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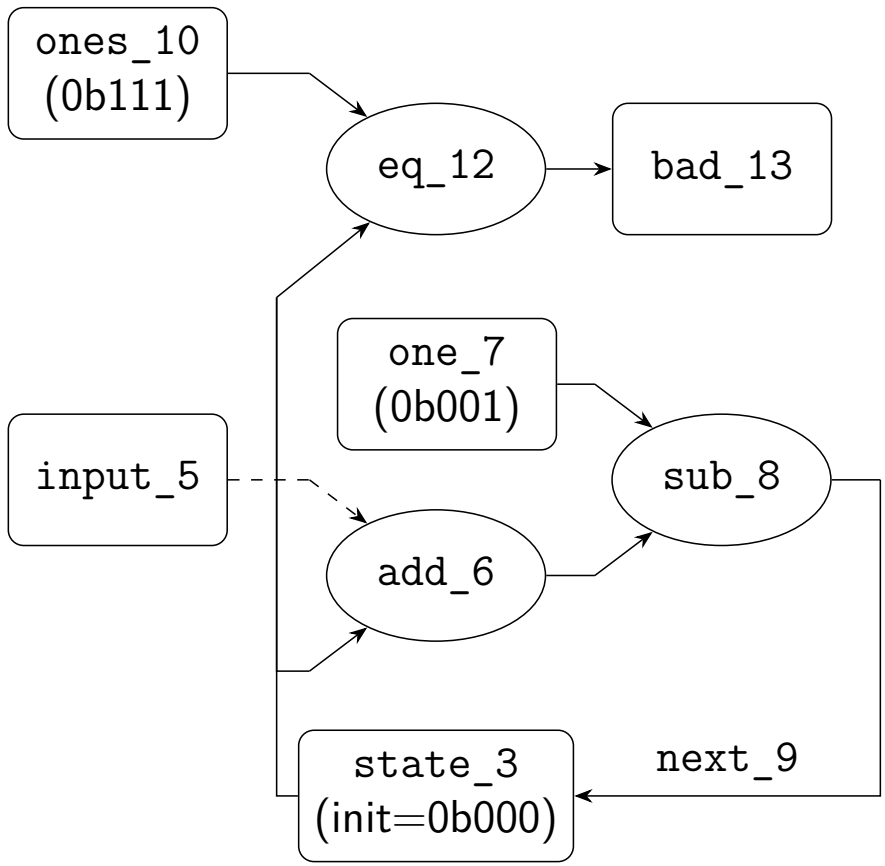

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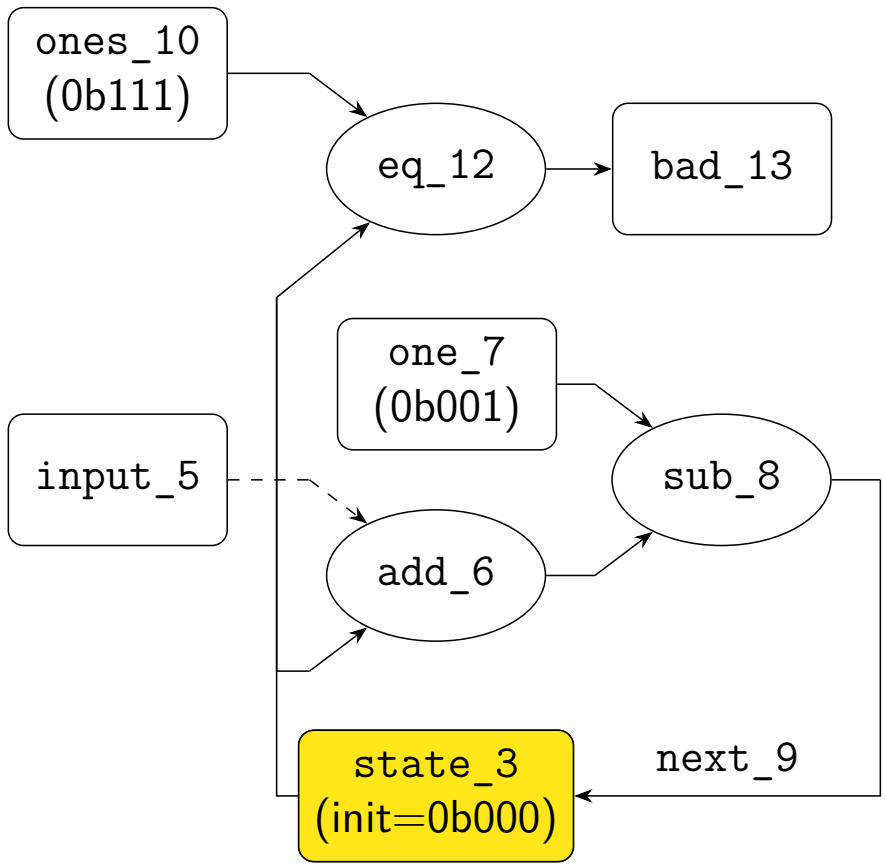

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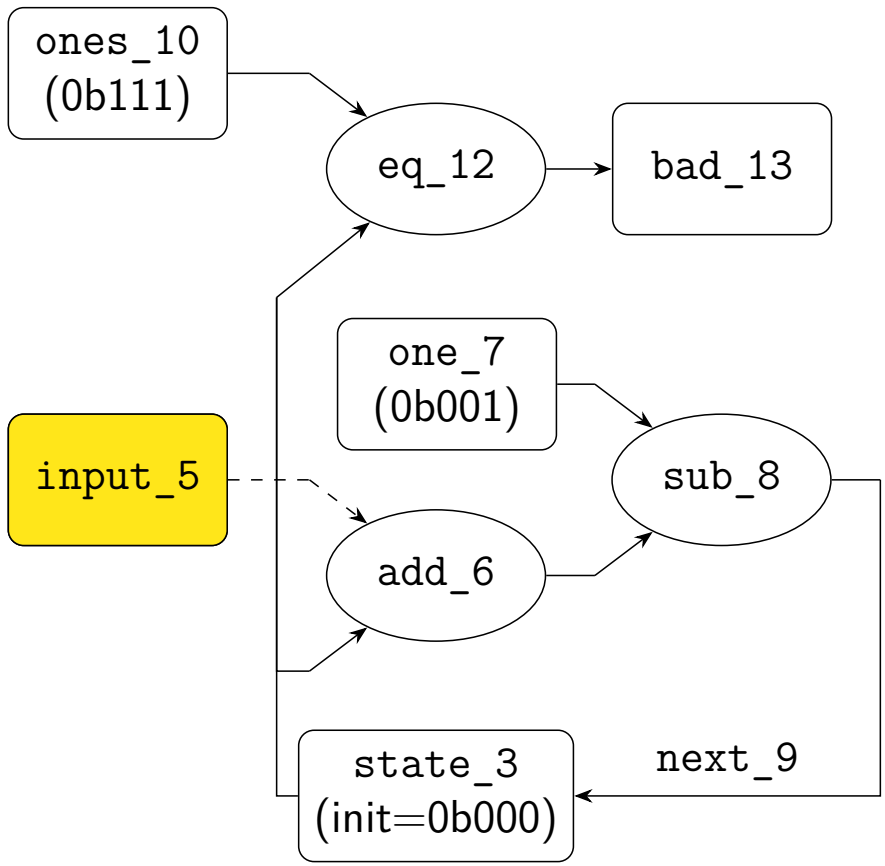

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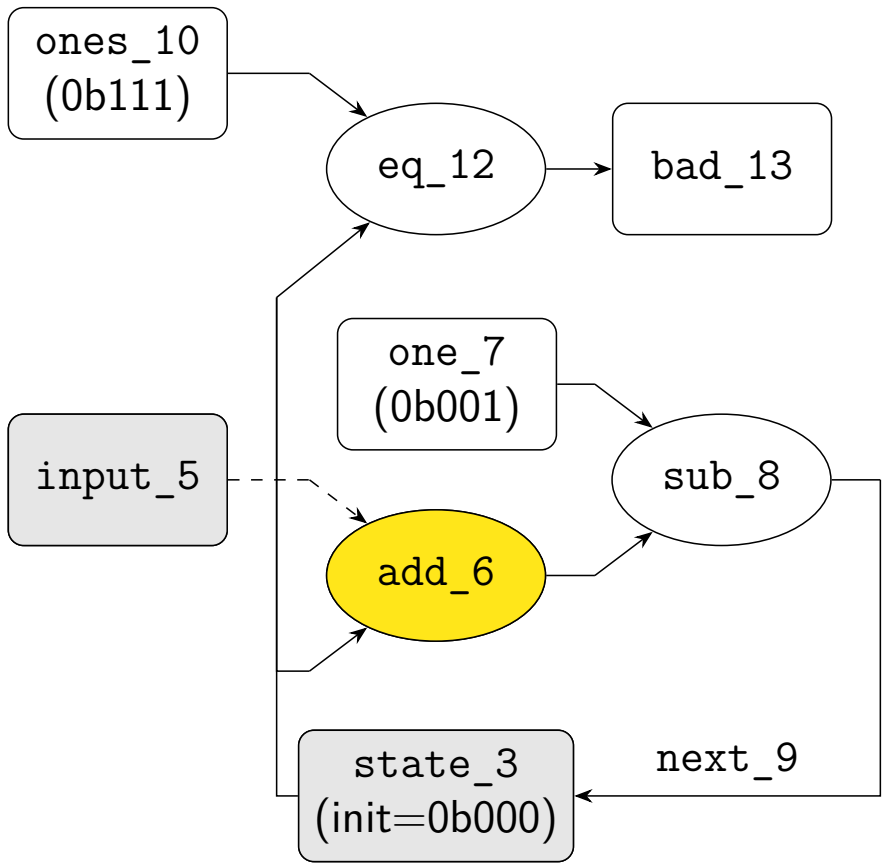

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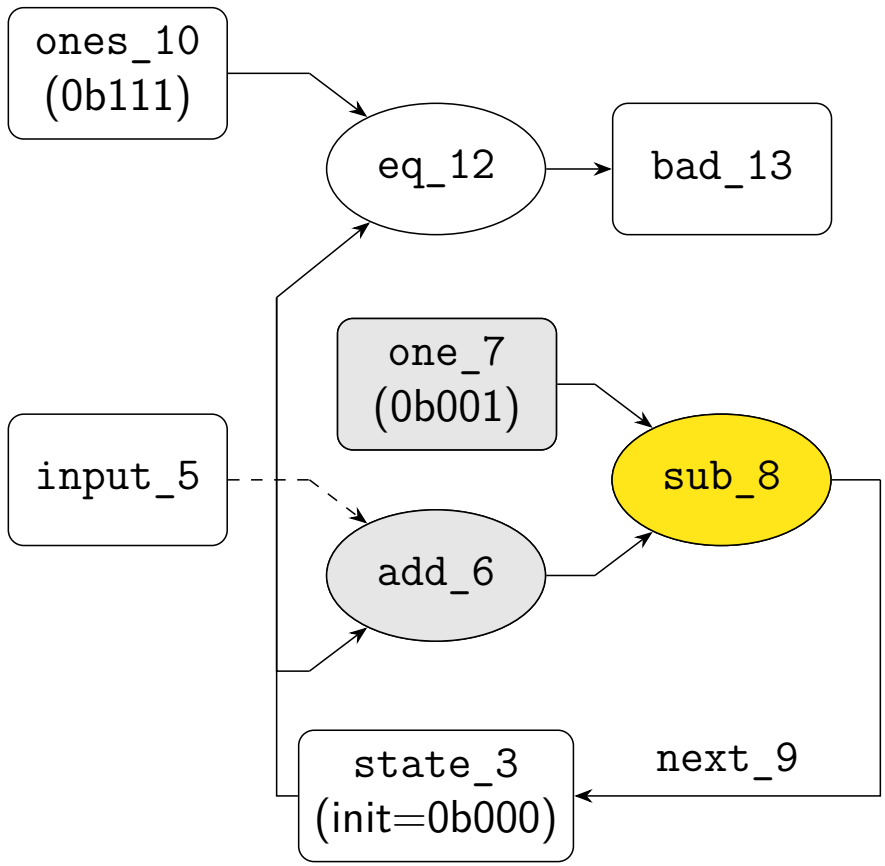

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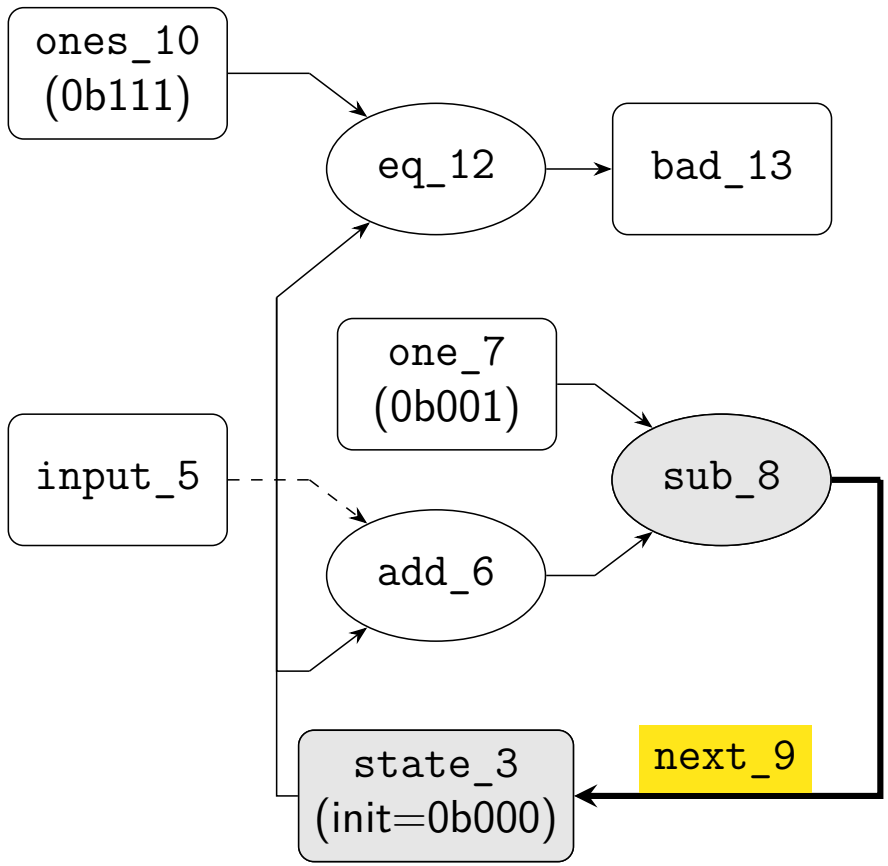

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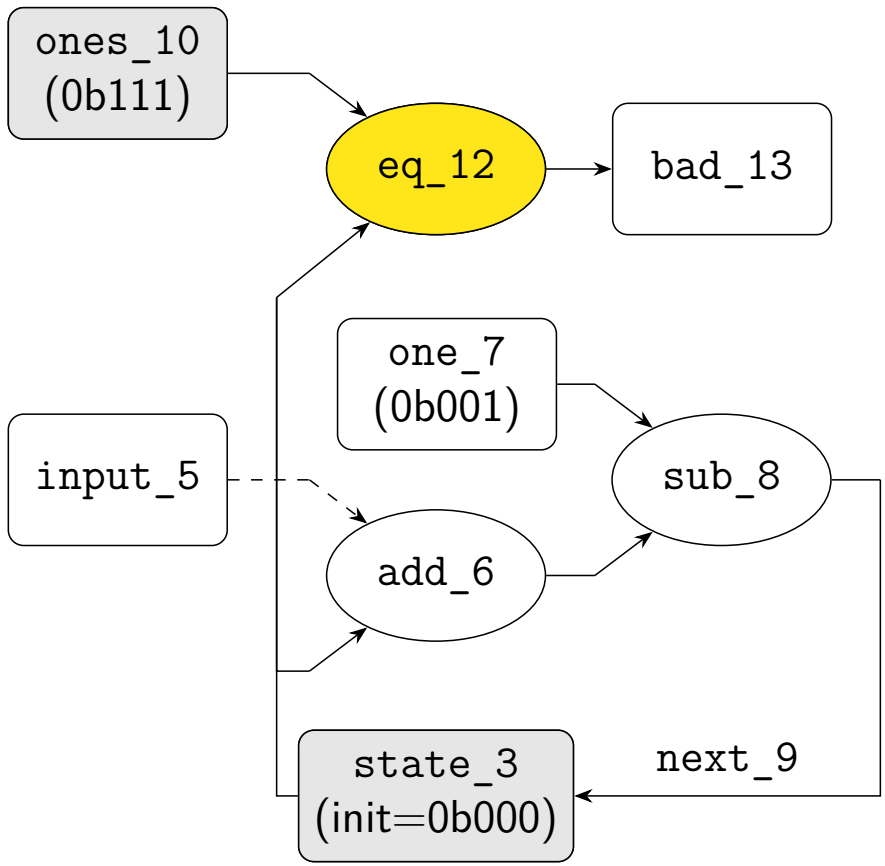

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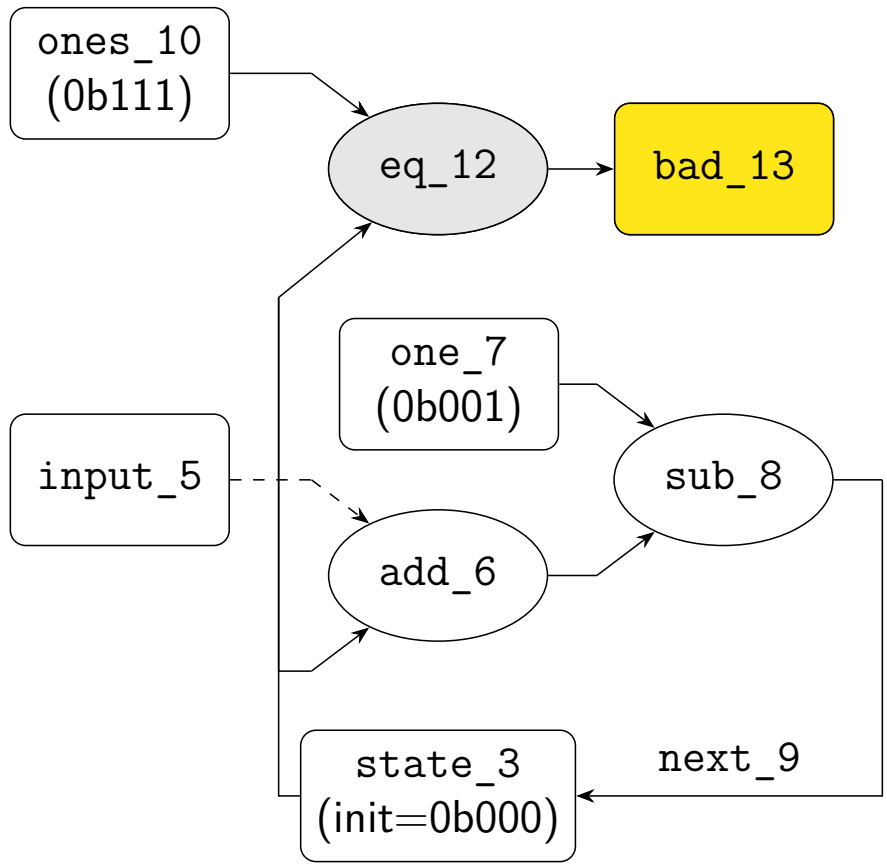

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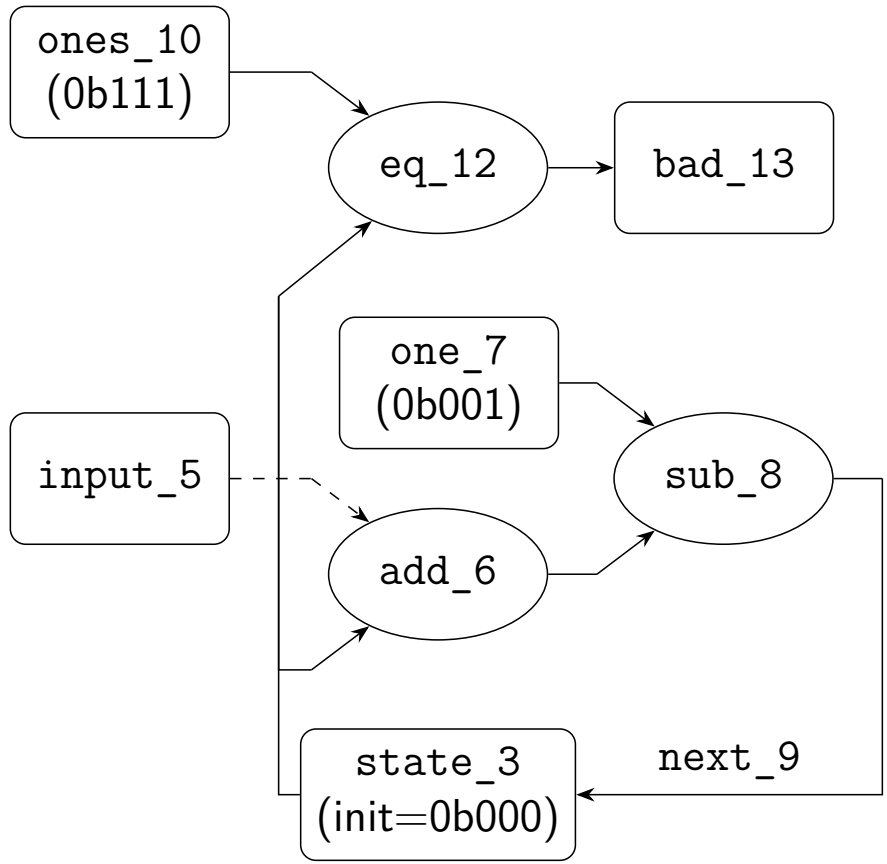

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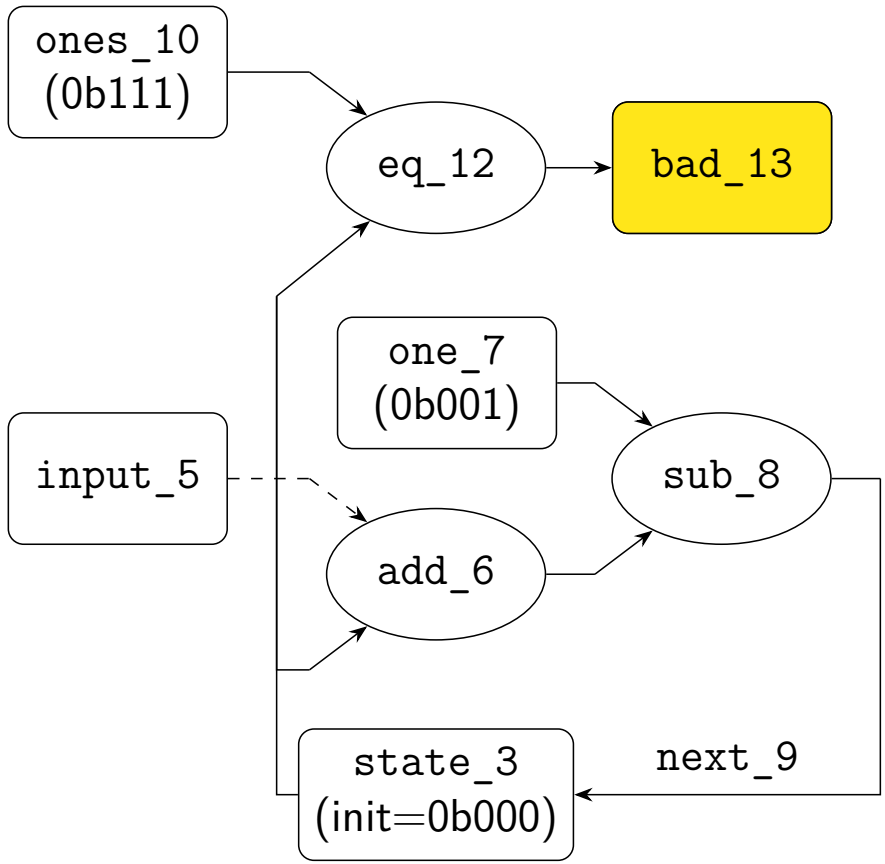

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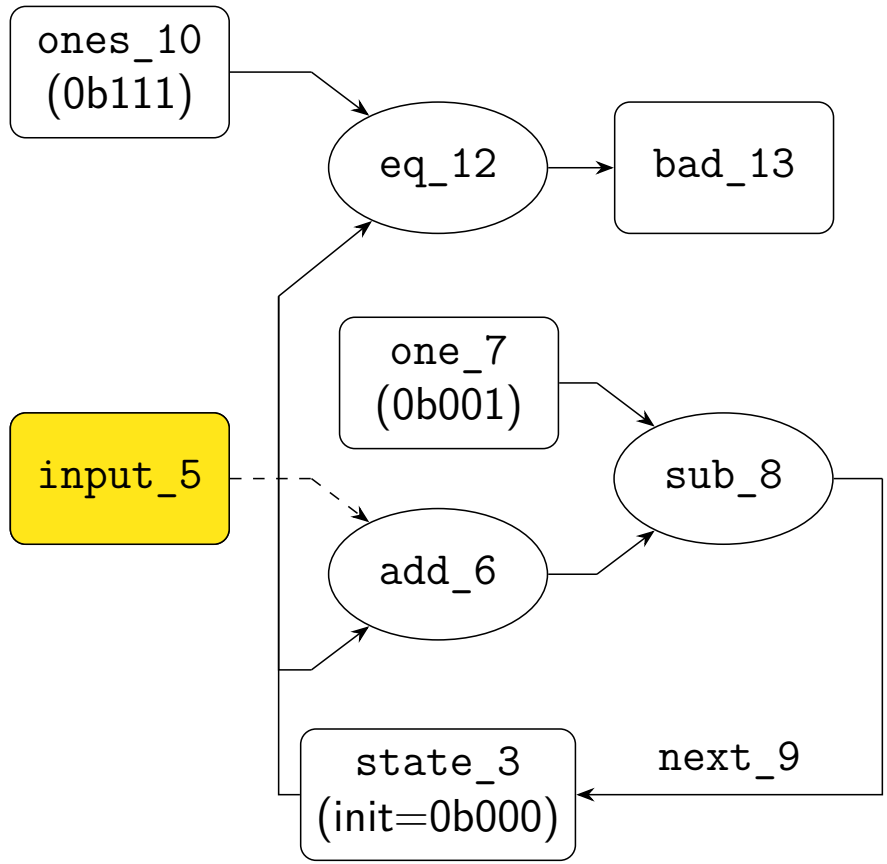

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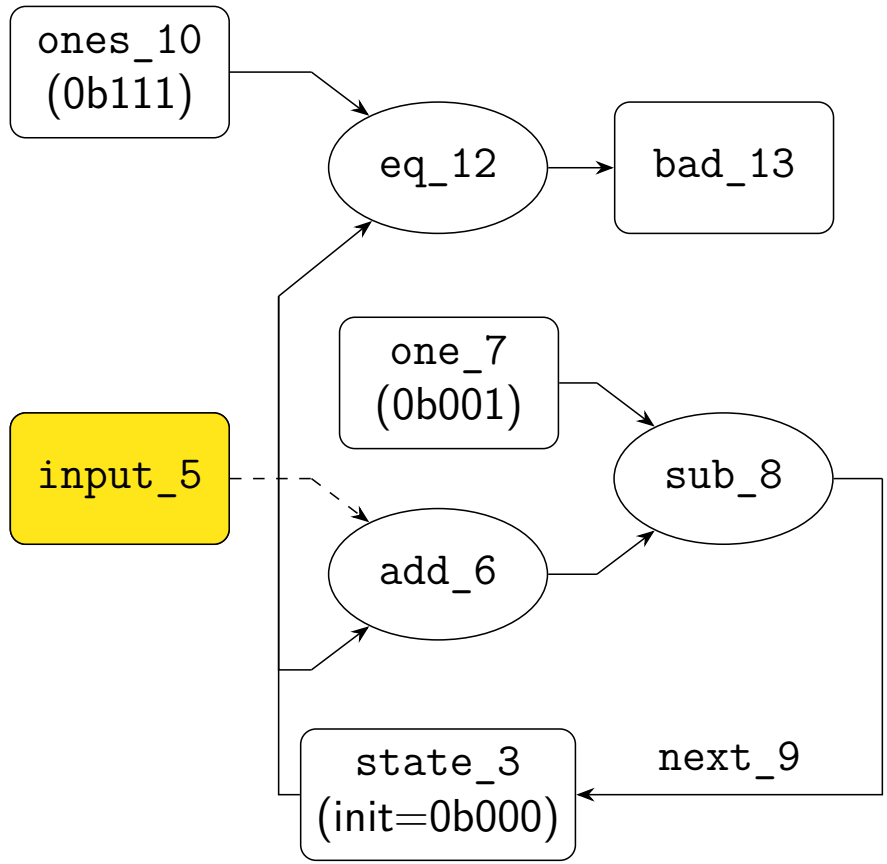

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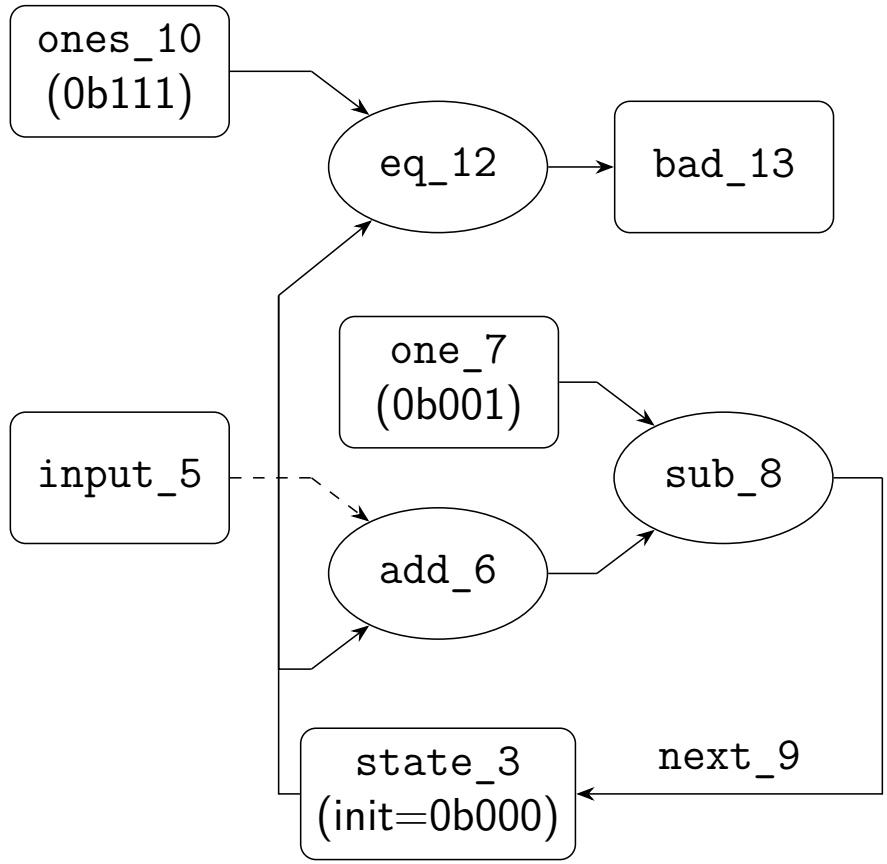
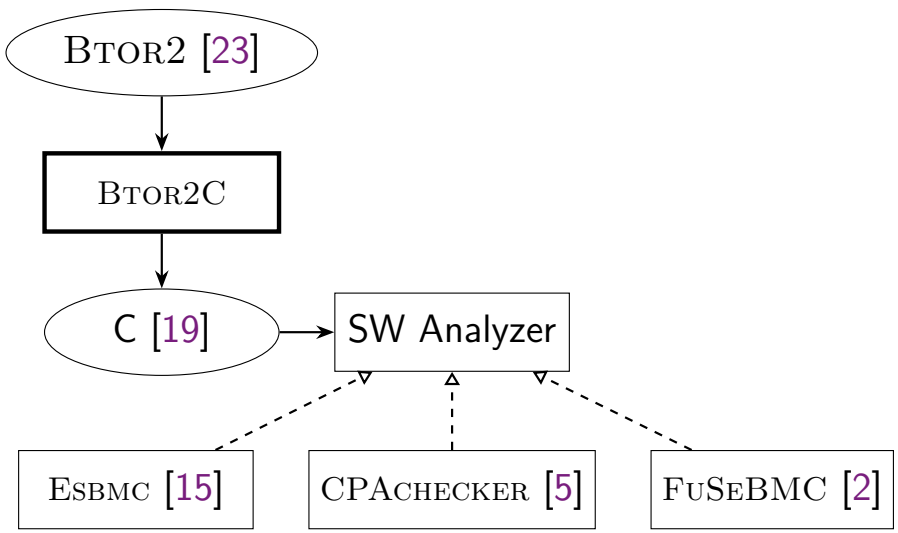



- A violation witness can be simulated by BTORSIM
- No format for **correctness witnesses** in BTOR2 [23]

# Btor2C: Translator from Btor2 to C [3]

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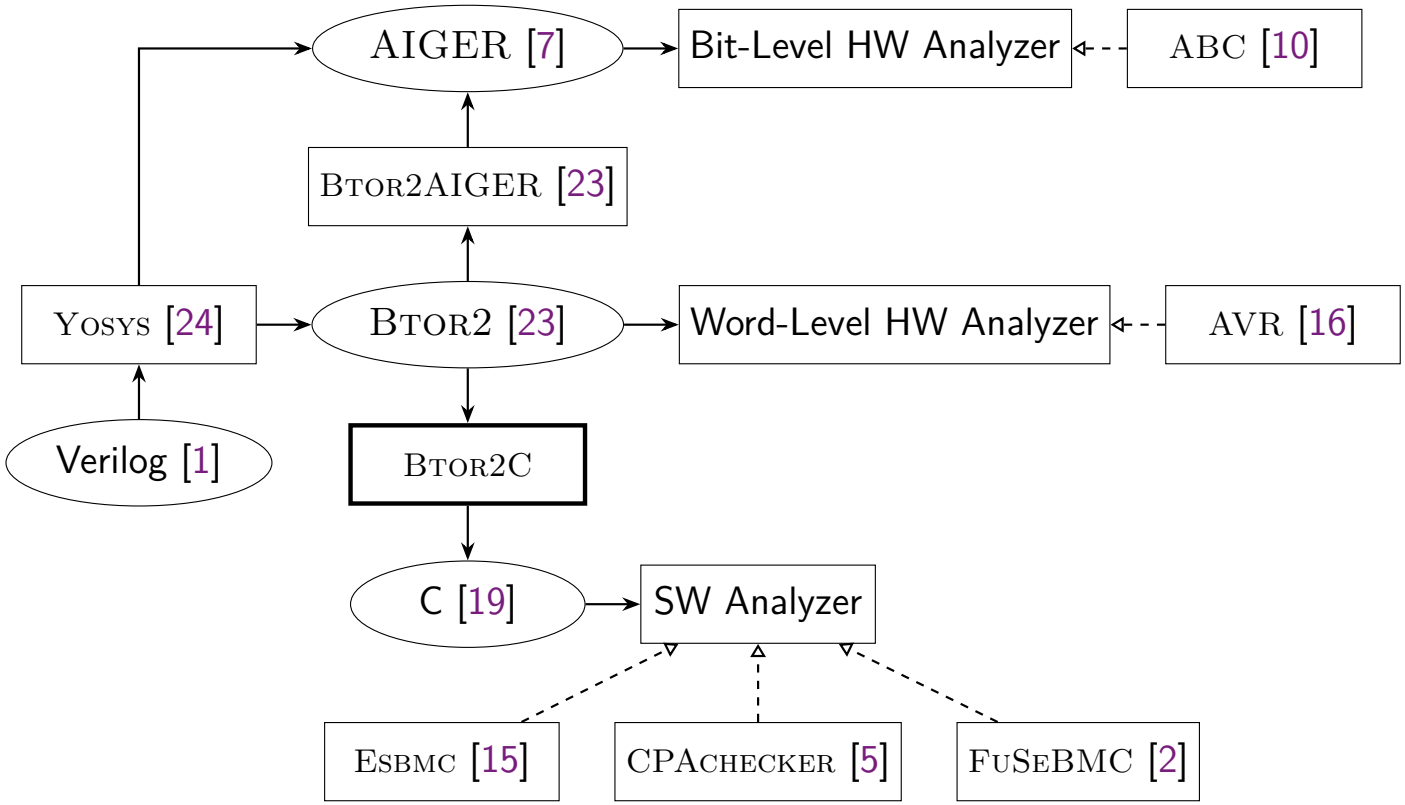


- Btor2 circuits translated to C programs[1]
- HW/SW tools compared on same tasks (and translations)

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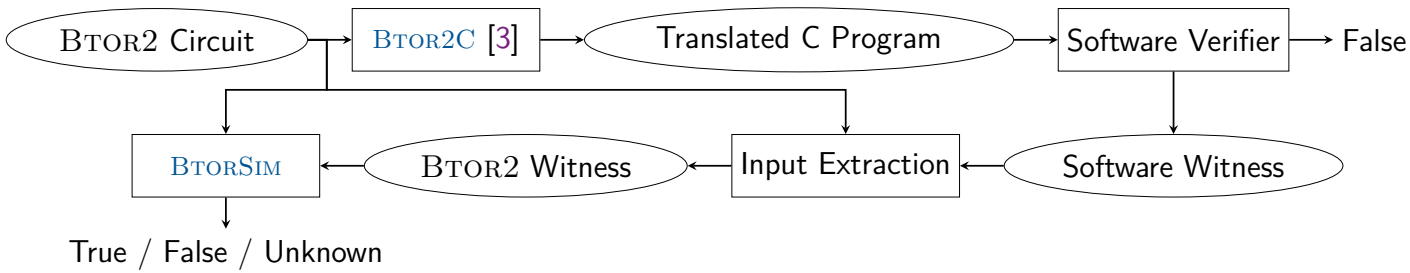
Translating software witnesses to Btor2 witnesses!

# Violation Witnesses



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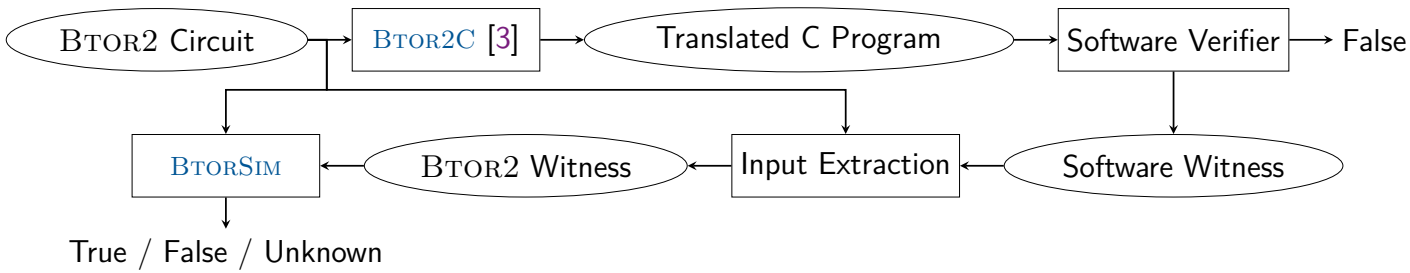


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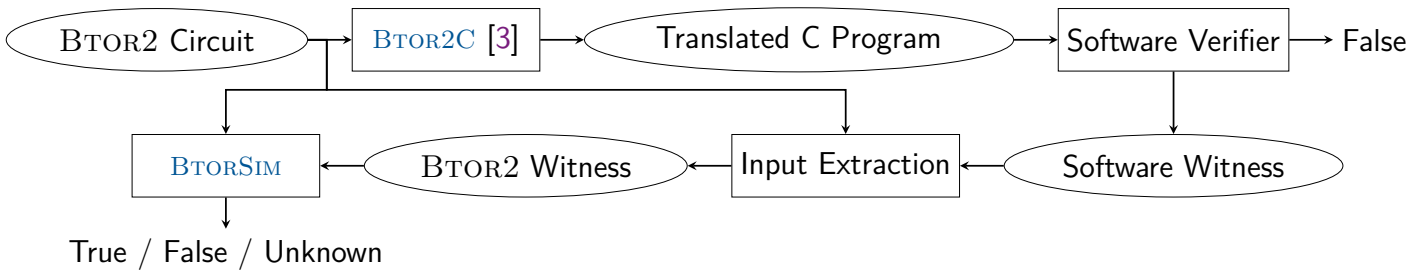


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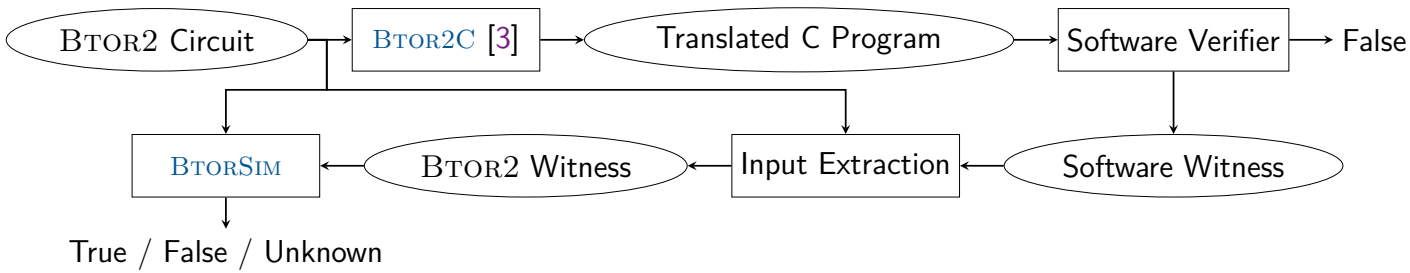


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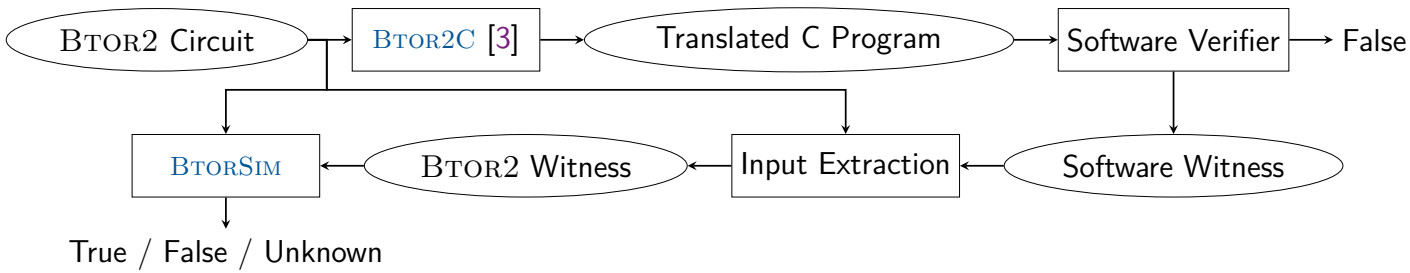


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- Simulate the circuit with BTORSIM [23]
  - Execution-based validation [4]

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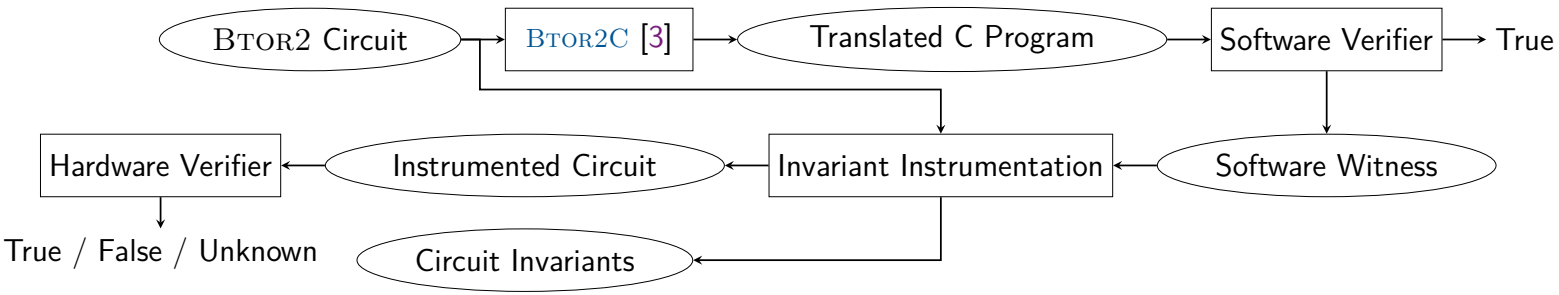

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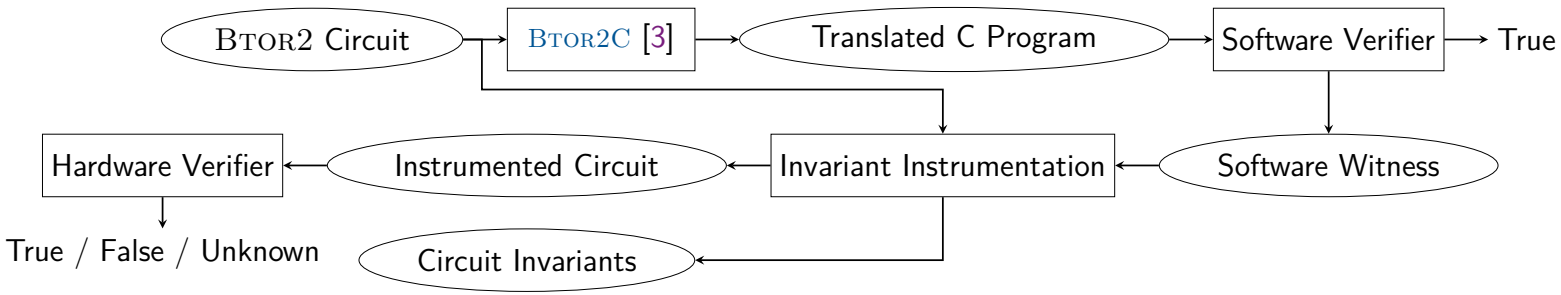


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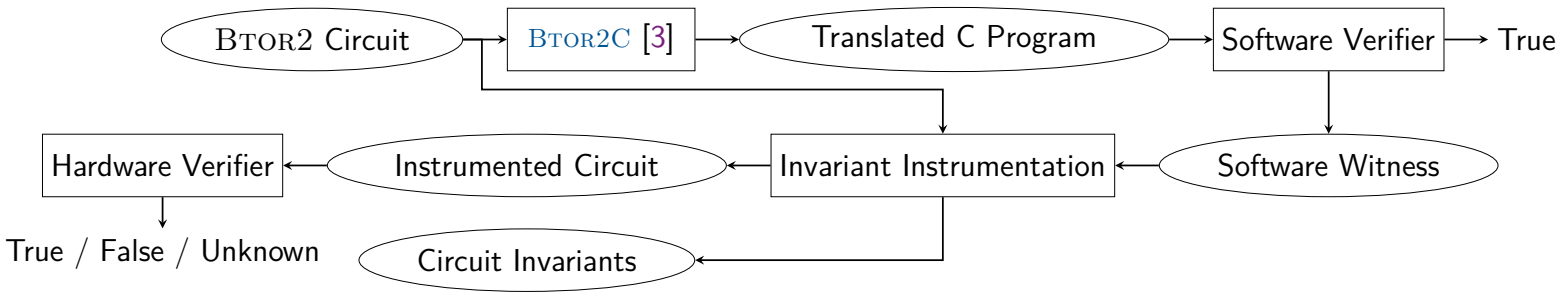


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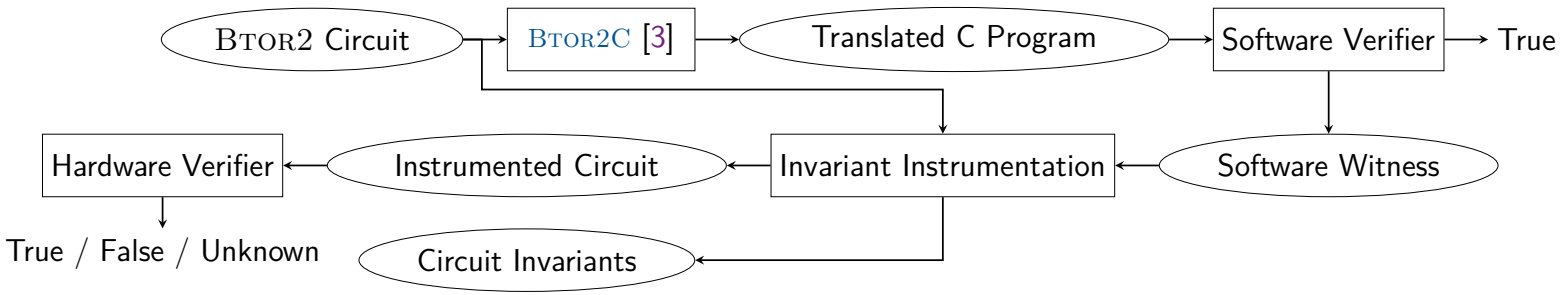


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- Validation via verification [6]
- Use hardware verifiers to validate software invariants

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  - Reject trivial invariants
  - Invariants related to property: re-establish proofs

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The reason BTOR2 has no format for correctness witnesses?

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